Application Note

DIGITAL OUTPUT TRANSDUCERS AND ∑Δ CONVERSION

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ABSTRACT

This application note supports users of LEM open-loop Hall effect current transducers in which analog to digital (A:D) conversion is performed with an on-board sigma-delta modulator giving a 1-bit serial Bitstream output. The transducers concerned include the HLSR xx-PW, HO xxx-NPW, HO xxx-SW and HO xxx-PW families. The addition of a sigma-delta modulator to the traditional accurate and compact analog transducers has many advantages: few connections are needed and the user completes the A:D conversion by choosing the filter used on the bitstream for the best compromise between resolution and response time, according to the application.

1. INTRODUCTION: LEM ADVANCED OPEN-LOOP TECHNOLOGY

LEM has a large family of analog open loop transducers in which Hall cell technology is integrated with dedicated signal processing to guarantee their accuracy and reliability. The transducers provide the smallest, lightest and most cost effective measurement solution while also having low power consumption.

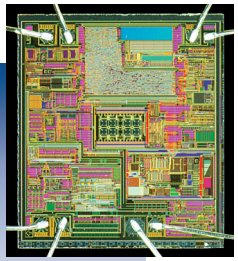


Fig. 2: LEM HG2 ASIC

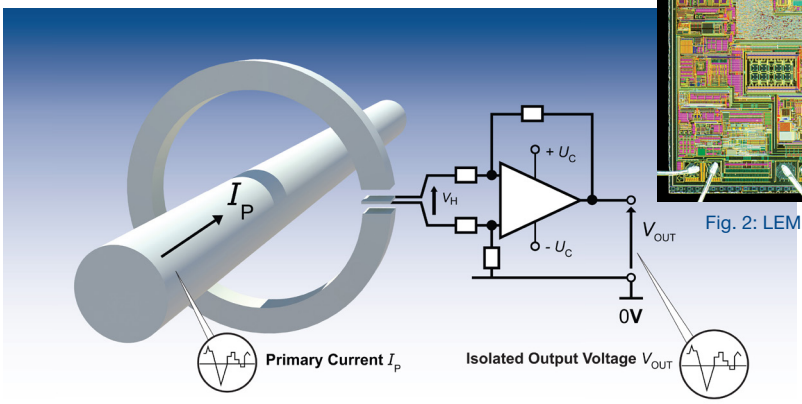


Fig. 1: Principle of Open-Loop technology

The principle is shown in figure 1: a primary current flowing in a conductor creates a magnetic field which is concentrated in the air gap of a magnetic circuit. The Hall cell output VH is proportional to the current measured. After signal processing the buffered output V_{OUT} is an exact analog representation of the primary current. To optimize performance the Hall cells and signal processing circuits are combined in a single CMOS ASIC (Application Specific Integrated Circuit).

2. LEM DIGITAL OPEN-LOOP TRANSDUCERS: OVERVIEW

LEM has made a significant step forward by adding a second order sigma-delta modulator to an improved ASIC used in a new family of transducers (figure 3). The transducer output is a bitstream where the density of 1's depends on the current measured, as illustrated in figure 4.

Fig. 3: HO xxx-NPW

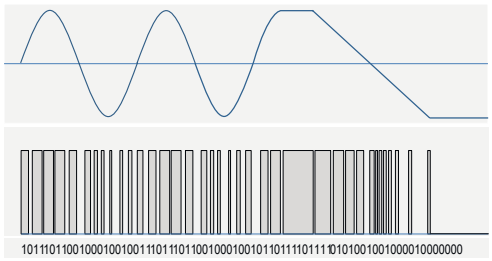


Fig. 4: Illustration of digital conversion with ∑Δ modulator

The detail of the transfer function is shown in figure 5. This shows the average density of 1's on a scale from 0 to 1, and the same output if it is filtered and represented as a 16-bit word on a scale from 0 to 65'535 (decimal). Figure 5 also show the equivalent output from an analog transducer. The performance of both transducer types is specified over the range +/- I_{PM}, corresponding to an average density of 1's from 0.1 to 0.9 for the digital transducer and an output voltage of 0.1 to 0.9 of the supply voltage for the analog type.

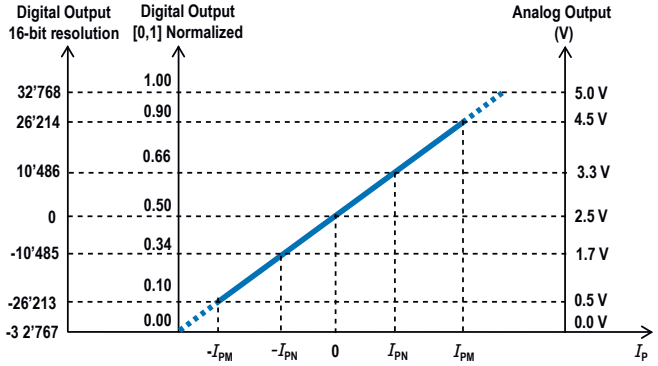


Fig. 5: Transfer function

The digital filter is implemented by the user, see figure 6. The advantage is that the number of connections to the transducer is minimized; each user can decide the filter(s) best suited to the application and the output format can be selected to match the system requirements.

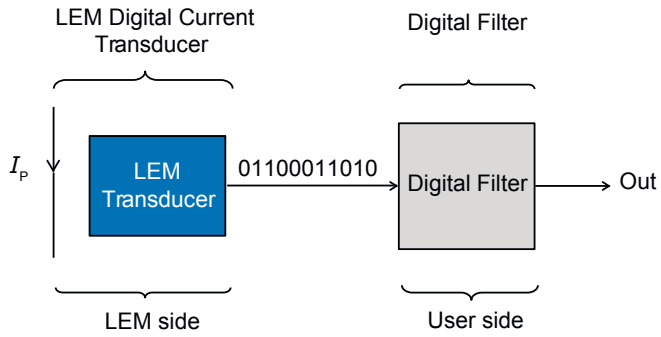


Fig. 6: LEM provides bitstream

3. ANALOG TO DIGITAL CONVERSION WITH ∑Δ MODULATORS

In general LEM current transducers are used either in control systems or measurement applications. When there is an analog output it is generally followed by conversion to a digital representation in order to use powerful control algorithms or for data storage. Including the A:D conversion in the transducer is therefore advantageous for the user in many applications.

A:D converters fall into 2 broad categories: 'Nyquist-rate' and 'oversampled'. In Nyquist-rate converters the analog input is sampled at a minimum rate of 2x the input frequency and the instantaneous value of the input is converted immediately to a digital word. In oversampled converters the sampling rate is higher. The number of bits in each sample may be reduced. In the case of the ∑Δ converters in the LEM transducers the analog input is typically sampled at 10.7 MHz and the digital output consists of a single bit. Therefore, in contrast to the Nyquist-rate converter, many samples must be used in a digital filter to know accurately the value of the input.

Oversampled converters offer many advantages over Nyquist-rate, on condition that the technology used allows a high enough clock frequency to permit oversampling:

i) They are well adapted to the inexpensive CMOS processes used in LEM transducers. The precision analog components needed for Nyquist-rate converters are not available; on the other hand, the high clock frequencies needed for oversampling can readily be generated;
ii) In all A:D converters there is quantization noise due to the difference between the quantized digital output and the exact value of the analog input. In ∑Δ converters this noise is pushed above the frequency of the sampled analog input;
iii) In the LEM families of transducers only the ∑Δ modulator which generates the single bit bitstream is implemented; the digital filter is provided by the user. This choice was made for two reasons:

a. As with traditional analog transducers, few connections are needed;
b. The user can optimize the digital filter – or more than one filter – according to the needs of a given application.

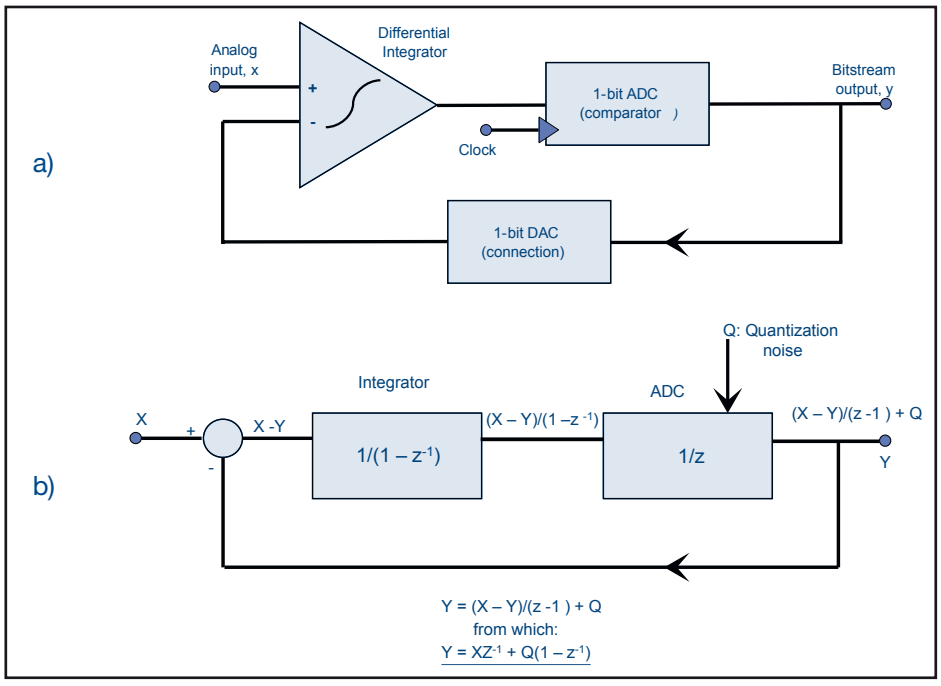


Fig. 7: first-order ∑Δ modulator

A first-order ∑Δ modulator is shown in figure 7a and its z-domain analysis in figure 7b. The output is the (delayed) input plus the quantization noise Q multiplied by (1 – z-1). The term in brackets is equivalent to differentiation, so quantization noise at low frequencies (in the signal band) is attenuated. The high frequency noise passed by differentiation will be removed in the user's digital filter.

LEM transducers use a second-order ∑Δ modulator in which a second first-order modulator is embedded at the position of the ADC of figure 7. This gives several performance advantages: for a detailed analysis the reader is referred to a standard text on the subject, such as reference (1).

4. FILTER AND PERFORMANCE CHOICES ON THE USER SIDE

As described above, LEM digital transducers output a bitstream containing noise whose filtered value corresponds to the analog input. The user processes the bitstream in a digital filter which rejects the high frequency noise.

The noise at different stages in the complete A:D process is shown in figure 8. At (a) there is always white noise from the analog front-end of the transducer, limited to half the sampling frequency. At (b) quantization noise is added, but only at high frequencies. (c) shows the output noise in an example in which the digital filter has a low cut-off frequency, which is good for precision; in this case the noise at the output is the same as when a traditional analog transducer is used with an equivalent filter. In (d) a wide band filter is used at the output, the response time is fast and the extra noise is not a drawback since this type of output is used to detect out-of-range currents. The versatility of the LEM digital transducers is due to being able to connect both the (c) and (d) filter types to the same bitstream.

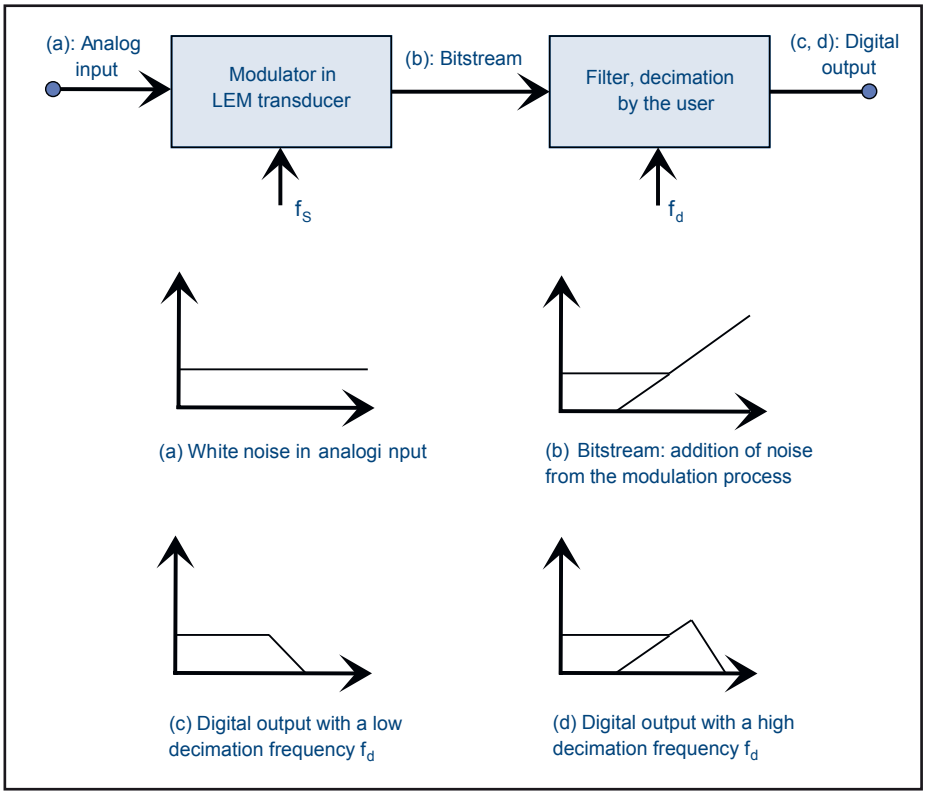


Fig. 8: Noise in the ∑Δ A:D conversion process.

Typically a sinc filter of order K is used. A first-order filter which has sampled N input bits gives as an output the average value of those bits; a Kth order filter is make by cascading K first-order filters – see reference 1. Figure 9 shows the frequency response of different sinc filters in which N = 384 bits and the bit rate is 10.7 Mb/s.

As with any filter, the order and bandwidth are chosen to optimize system performance. A narrow bandwidth gives lowest noise (or highest resolution) at the expense of response time, and vice versa. In the example of figure 10 the bitstream is processed twice: in a 20 kHz filter which gives a resolution of 12 bits for accurate measurement of the primary current and in a wideband filter to detect excess currents with a response time of 5 µs. Additionally the transducer internal OCD (over current detect) output allows detection of short circuits with a response time of only 2.7 µs.

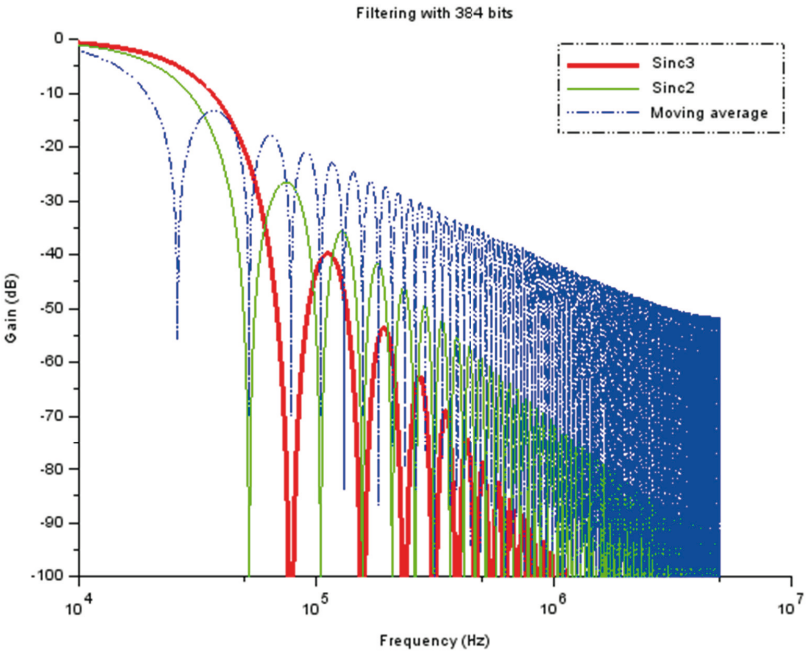


Fig. 9: Response of different sinc filters.

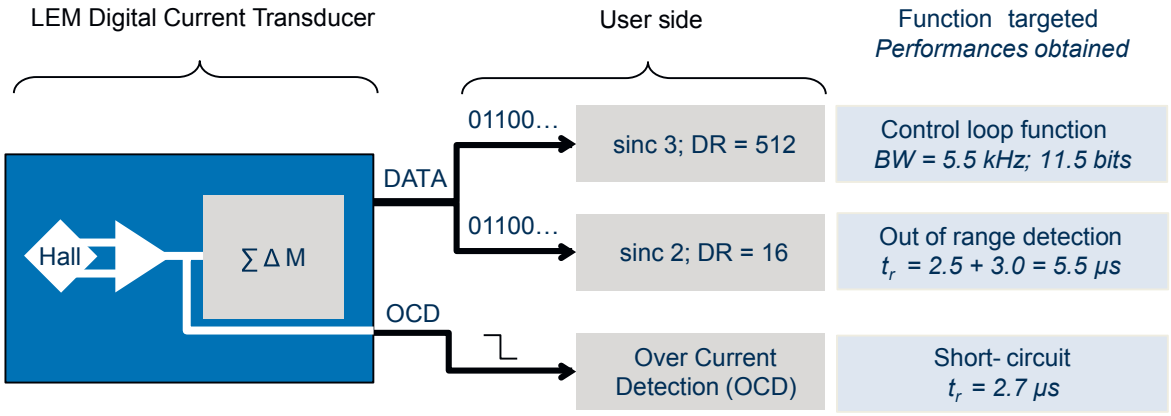


Fig. 10: Application example with Decimation Ratio and filter order: influence on response time and resolution

Packets of N bits are sampled one at a time and processed with some previous packets in the digital filter. Due to the high modulator oversampling ratio, the digital filter output can be processed every N bits with no loss of information within the band of interest. An output from the filter may be obtained after every N bits, and N, equal to fs/fd in figure 8, is known as the Decimation Ratio (DR).

The latency of filter depends on its architecture. Take a simple case where the output is sampled after each packet of N bits. For a clock period T_{CLK} the output is delayed by 2 x DR x T_{CLK} for a sinc2 and 3 x DR x T_{CLK} for a sinc3 filter. In table 1 the bit rate at the transducer output is 10.7 Mb/s, so T_{CLK} is 0.1 us. The combination of DR, filter choice and bit rate leads to the response time, the bandwidth and the effective resolution of each of the signal paths connected to the bitstream. The response times are somewhat faster than the delayed output given above. Partly this is because the standard LEM definition has been used, where the response time is between 90% of the input and output signals. It is further improved by reading the filter output continuously, instead of sampling it after each packet of N bits.

SINC K Order	Bit rate Mb/s	Over Sampling Ratio (DR)M	Product response time (µs)	Filter Response time (µs)	Over Current Detection (OCD) (µs)	Filter bandwidth -3dB (kHz)	LEM effective resolution (Bit)	Comments
31	0.7	10242	.5	287.1	2.72	.7	12.0	Better accuracy
		5122	.5	143.6	2.75	.5	11.5	
		2562	.5	71.8	2.71	1.0	10.9	
		1282	.5	35.9	2.72	1.9	10.3	
		64	2.51	7.92	.7	43.8	9.8	
		32	2.59	.0	2.78	7.6	8.7	
		16	2.54	.5	2.7	175.2	7.3	
		82	.5	2.22	.7	350.4	5.7	
21	0.7	10242	.5	191.4	2.73	.3	11.9	Better response time
		5122	.5	95.7	2.76	.7	11.3	
		2562	.5	47.9	2.71	3.3	10.7	
		1282	.5	23.9	2.72	6.7	10.1	
		64	2.51	2.02	.7	53.3	9.4	
		32	2.56	.0	2.7	106.7	8.1	
		16	2.53	.0	2.7	213.3	6.4	
		82	.5	1.52	.7	426.7	4.7	
11	0.7	10242	.5	95.7	2.74	.3	9.2	Fast response time
		5122	.5	47.9	2.78	.7	8.3	
		2562	.5	23.9	2.71	7.3	7.3	
		1282	.5	12.0	2.73	4.6	6.3	
		64	2.56	.0	2.76	9.2	5.2	
		32	2.53	.0	2.7	138.4	4.2	
		16	2.51	.5	2.7	276.9	3.3	
		82	.5	0.72	.7	553.7	2.5	

Table 1: HO 150-NPW performances: Performance = f (DR, SINC K FILTER, BANDWIDTH)

The resolution of the complete system including the analog part of the transducer, the sigma-delta modulator and the digital filter is limited either by the quantization noise inherent to the system or by the analog noise from the Hall cells and amplifiers. For fast response times (for example with a DR = 16 and a sinc2 filter) the resolution is defined by the system and will be the same with any transducer. If the filter is changed to sinc3 and the DR is increased the effective resolution is improved but will be limited to 11 – 13 bits (depending on the sensor sensitivity) by analog noise. The term "Effective" resolution is used because for system convenience the filter may output a word with a length of 16 bits or 2 x 8 bits. However only the most significant bits corresponding to the effective resolution contain useful information, the less significant bits contain noise.

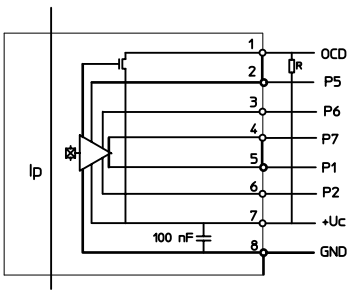
The filters used with LEM transducers may be implemented in DSP circuits or microprocessors, giving the user complete flexibility in the design choice.

5. PHYSICAL INTERFACES

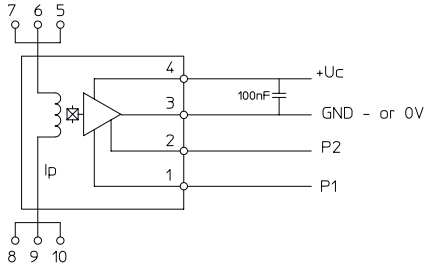
To transmit the bitstream LEM offers the choice between several physical interfaces. They fall into 3 categories:

i) Single-ended, see section 5.1;
ii) Differential Manchester, see section 5.2;
iii) Fully differential clock and data, see section 5.3.

In all cases the bit rate is 10.7 Mb/s if the internal clock of the transducer is used. If an external clock is used the frequency range of 5 – 10.1 Mhz or 11.4 - 12.5 MHz is allowed, with the restriction that 10.7 MHz must be avoided (see the transducer datasheet for details).



Connection diagramm for HO xxx_PW; SW & NPW



Connection diagramm for HLSR xx-PW

5.1 2W CMOS (Single-ended)

Clock and data are single-ended CMOS levels (UC and GND); the clock may be an input or an output. This is suitable for short connections, up to some 10's of centimeters, above which EMC issues may become important. The maximum allowed capacitive load is 30 pF. The pin allocation for an HLSR xx-PW, HO xxx-NPW, HO xxx-PW, HO xxx-SW transducer is shown in Table 2 and the timing diagram in figure 10.

		Pin Name							
Configuration	Product Name	GND	$+U_C$	P2	P1	P7	P6	P5	OCD
2W CMOS (Single-ended) CLK Out	HO xxx-NPW-X0XX HO xxx-PW-X0XX HO xxx-SW-X0XX	GND	$+U_C$	D_{out}	CLK	NC	NC	GND or NC	OCD
	HLSR xx-PW-X0X	GND	$+U_C$	D_{out}	CLK	-	-	-	-
2W CMOS (Single-ended) CLK In	HO xxx-NPW-X8XX HO xxx-PW-X8XX HO xxx-SW-X8XX	GND	$+U_C$	D_{out}	CLK	NC	NC	GND or NC	OCD
	HLSR xx-PW-X8X	GND	$+U_C$	D_{out}	CLK	-	-	-	-

Table 2: 2W CMOS (Single-ended) wiring

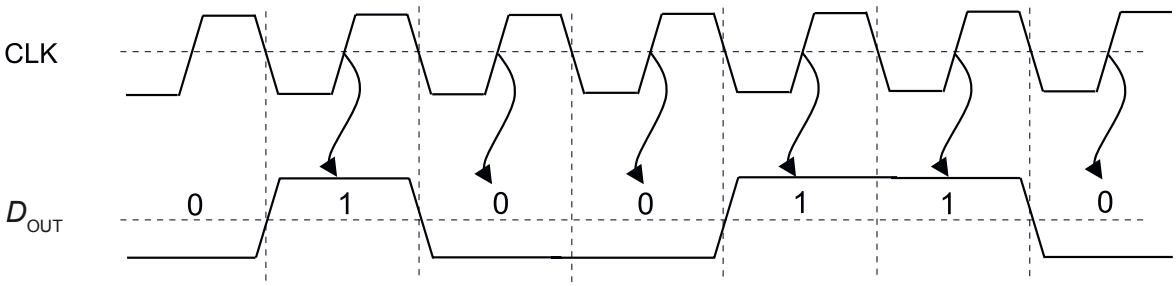


Fig. 11: 2W CMOS (Single-ended)

5.2 2W RS422 or LVDS Manchester (IEEE 802.3) differential signals

This interface is suitable for transmission over longer distances in transducers where only two output connections are available. In this case the clock and data are combined as a Manchester coded signal. This is output on one transducer pin (P2) and its complement on another (P1). The differential signal thus generated is compatible with the RS422 or LVDS standards. By keeping the two signal tracks physically close, EMC effects - both transmitted and received - can be kept to a low level. The pin allocation for both transducer families is shown in Table 3 and the timing diagram in figure 12.

		Pin Name							
Configuration	Product Name	GND	$+U_C$	P2	P1	P7	P6	P5	OCD
RS422 MANCHESTER	HO xxx-NPW-X1XX HO xxx-PW-X1XX HO xxx-SW-X1XX	GND	$+U_C$	D_{out}	CLK	NC	NC	GND or NC	OCD
	HLSR xx-PW-X1X	GND	$+U_C$	D_{out}	CLK	-	-	-	-
LVDS MANCHESTER	HO xxx-NPW-X3XX HO xxx-PW-X3XX HO xxx-SW-X3XX	GND	$+U_C$	D_{out}	CLK	NC	NC	GND or NC	OCD
	HLSR xx-PW-X3X	GND	$+U_C$	D_{out}	CLK	-	-	-	-

Table 3: Manchester interfaces wiring

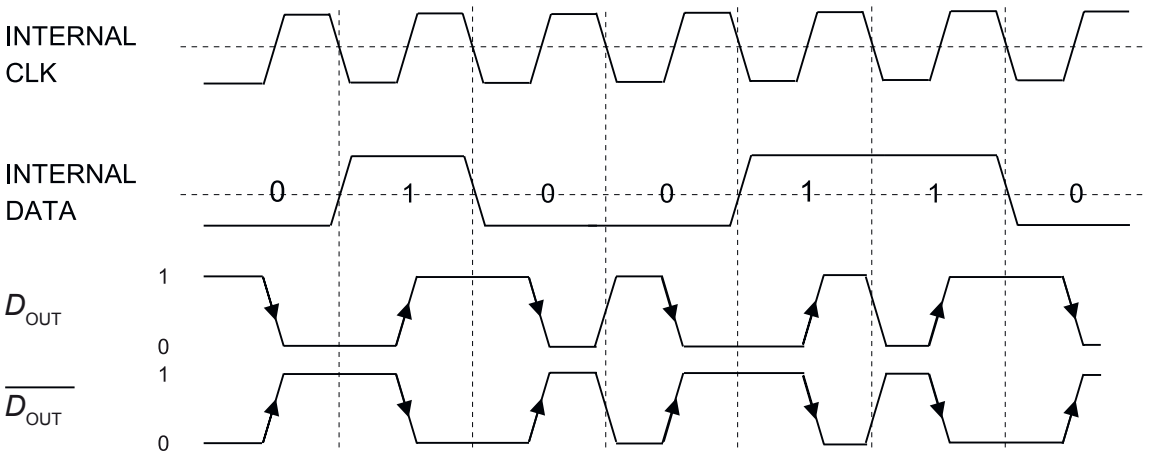


Fig. 12: Manchester coded data

With a RS422 output the 1 and 0 levels are nominally U_C and GND respectively and the connections are not loaded, unless a load is needed for matching. With an LVDS output the common mode voltage is nominally 1.25 V and the differential voltage is 350 mV peak. A floating 100 ohm load must be provided between the differential D_{OUT} signals.

One disadvantage however with a Manchester coded signal is that clock and data must berecovered at the receiver side. This can be done in a FPGA or a DSP with dedicated hardware blocks.

5.3 4W CLK Out and CLK In; RS422, with direct connection and with capacitor coupling, and LVDS standards.

In the HO xxx-NPW, HO xxx-SW AND HO xxx-PW transducers both clock and data are available as differential signals. The transducers can be configured such that the signals are compatible with the RS422 or LVDS standards. As with the differential Manchester output these formats create little EMC interference. The earlier timing diagram of figure 11 applies also to these interfaces. The 1 and 0 levels described for RS422 and LVDS in Section 5.2 also apply.

When the common mode level between 0.35 x U_C and 0.75 U_C, an external clock is provided for the LEM transducer in RS422 mode ('CLK IN') a direct connection to the clock pins may be made. If the absolute values of the incoming signal are not known the clocks may be connected with a capacitor coupling and the LEM transducer will provide the correct common-mode voltage.

		Pin Name							
Configuration	Product Name	GND	$+U_C$	P2	P1	P7	P6	P5	OCD
4W RS422 CLK Out	HO xxx-NPW-X4XX HO xxx-PW-X4XX HO xxx-SW-X4XX	GND	$+U_C$	D_{out}	$\overline{D_{out}}$	$\overline{CLK}$	CLK	GND or NC	OCD
4W RS422 CLK In (Mode C)	HO xxx-NPW-XCXX HO xxx-PW-XCXX HO xxx-SW-XCXX	GND	$+U_C$	D_{out}	$\overline{D_{out}}$	$\overline{CLK}$	CLK	$+U_C$	OCD
4W RS422 CLK In (Mode D)	HO xxx-NPW-XDXX HO xxx-PW-XDXX HO xxx-SW-XDXX	GND	$+U_C$	D_{out}	$\overline{D_{out}}$	$\overline{CLK}$	CLK	$+U_C$	OCD
4W LVDS CLK Out	HO xxx-NPW-X2XX HO xxx-PW-X2XX HO xxx-SW-X2XX	GND	$+U_C$	D_{out}	$\overline{D_{out}}$	$\overline{CLK}$	CLK	GND or NC	OCD
4W LVDS CLK In	HO xxx-NPW-XAXX HO xxx-PW-XAXX HO xxx-SW-XAXX	GND	$+U_C$	D_{out}	$\overline{D_{out}}$	$\overline{CLK}$	CLK	$+U_C$	OCD

Table 4: 4W RS422 or LVDS, CLK Out and CLK Inconnections

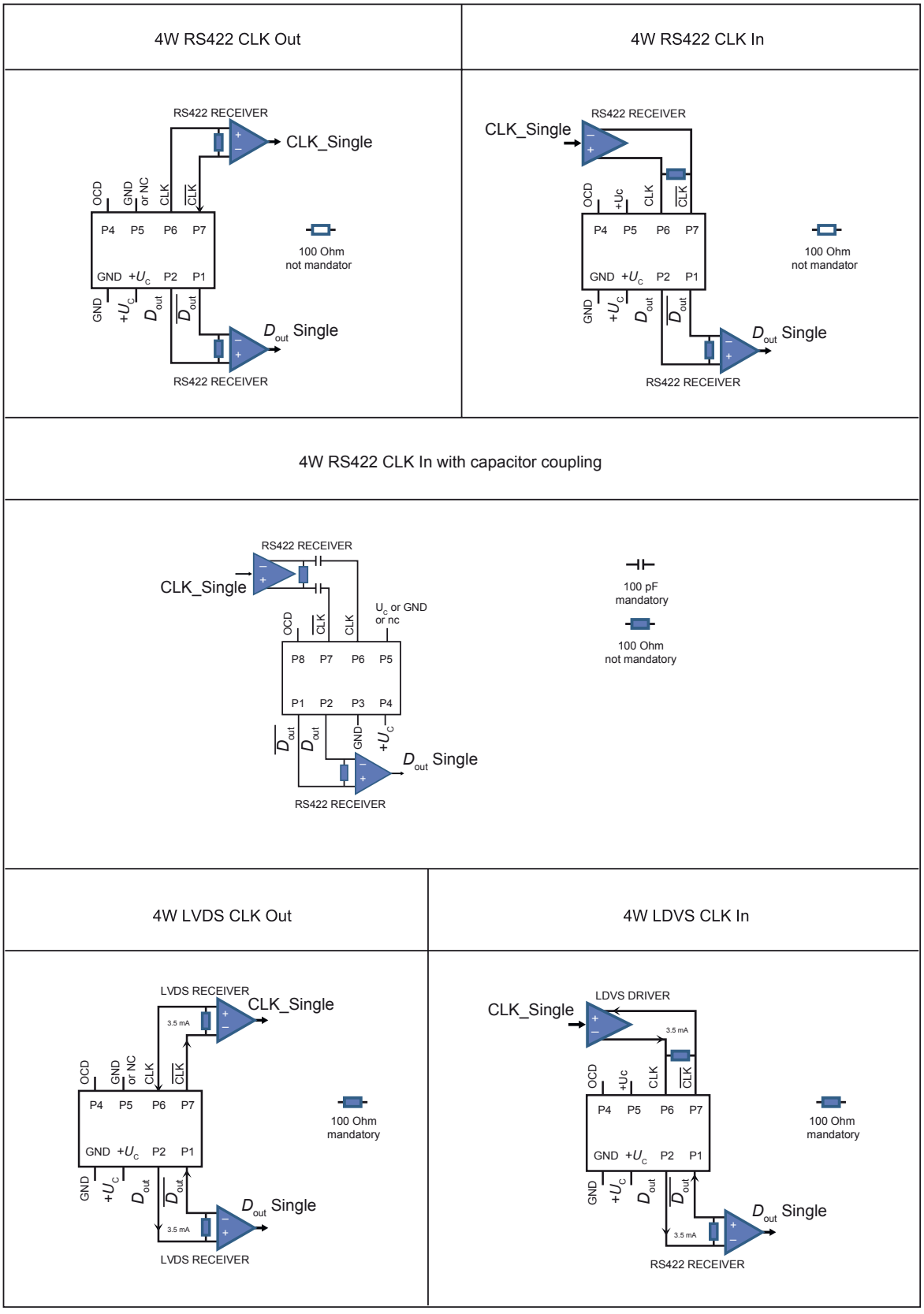


Fig. 13: Four wire RS422 and LVDS interfaces. The load resistors are optional in all the RS422 examples.

6. DELAY VS FILTER: EXAMPLE

As described in section 4, the combination of DR, filter choice and bit rate determines the response time, the bandwidth and the effective resolution of each of the signal paths connected to the bitstream.

The following simulations illustrate this trade-off in the time domain to optimize system performance: a narrow bandwidth gives lowest noise (or highest resolution) at the expense of response time, and vice versa.

The “digital delay” between the primary signal and the output signal due the filter is constant in each case. This property makes easy to correct for the delay by shifting the signal in time.

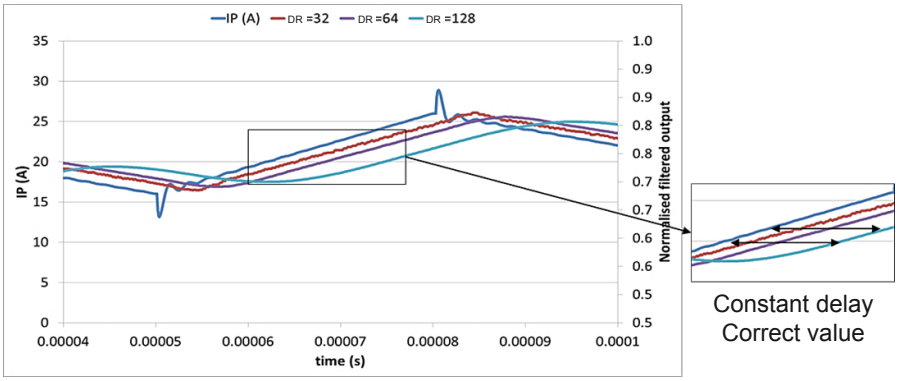


Fig. 14: Simulation Filter (sinc2), DR vs. Delay

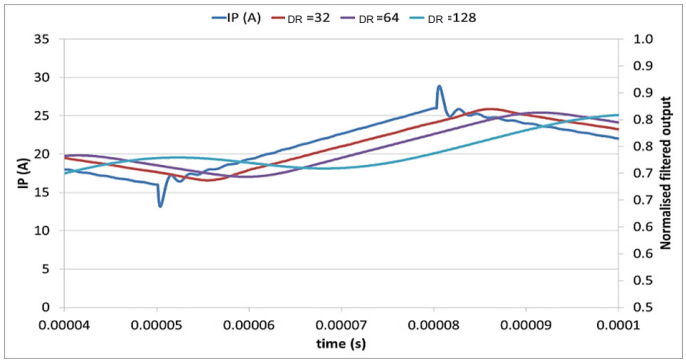


Fig. 15: Simulation Filter (sinc3), DR vs. Delay

7. REFERENCES

(1): Understanding Delta-Sigma Data Converters’; Schreier and Temes; Wiler Interscience; ISBN 0-471-46585-2.