GXN & GXS APPLICATION NOTES

INFORMATION IN THIS DOCUMENT SHOULD BE USED AS REFERENCE, THEY ARE NOT GUARANTEED VALUES

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1 Revision history

Rev	Date	Who	Change and updates
0	11/Nov/2025	JCX	Creation

2 CLARIFICATION

- LEM offer a wide range of ICS products in different packages and configurations. Customers can choose between different supply voltages, output type (referenced or ratiometric), voltage reference (internal or external), Over Current Detection (internally or externally set). The goal of this application note is to help customers to design their schematics according to the chosen functionalities.
- Information in this document should be used as reference; they are not guaranteed values.

3 Typical Application Circuit

3.1 GXS ANF- SOIC8

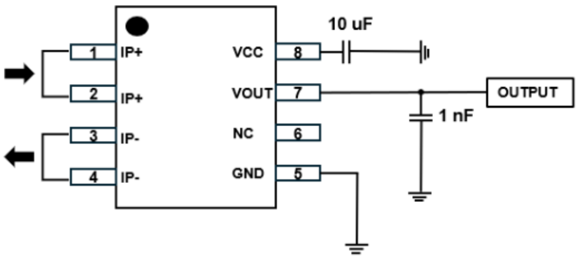


Figure3.1 Ratiometric mode application circuit

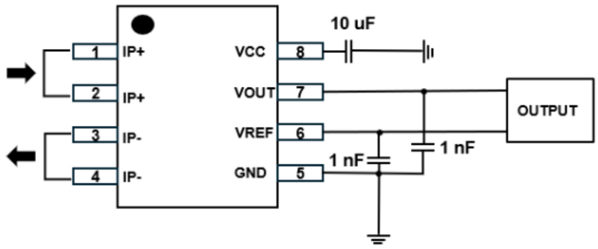


Figure3.2 Fixed mode application circuit

3.2 GXN ANC/AND-SOIC16

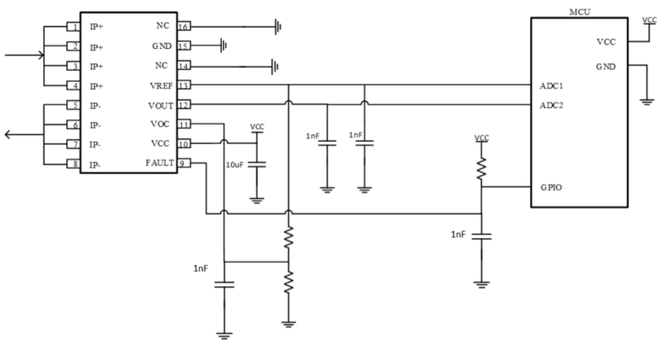


Figure3.3 GXN_ANC Fixed output mode

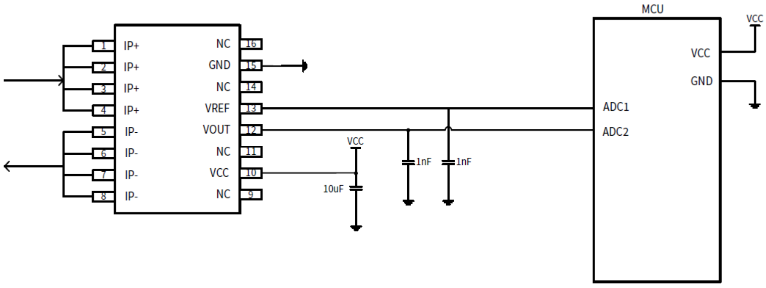


Figure3.4 GXN_AND Fixed output mode

4 Thermal Resistior

4.1 Aim

- Aim to clarify GXS ANF and GXN Series thermal performance. Monitor the junction temperature T_j to ensure it does not exceed the maximum value T_{jMAX} , preventing permanent circuit damage.

4.2 Definition

- Thermal Resistor is a metric that measures the degree to which an electronic component or material impedes heat conduction. In semiconductor integrated circuits, it is commonly used to evaluate the ability of the die within the package to conduct heat generated by the die to the circuit board or surrounding environment, assuming the die is the primary heat source within the system. $R_{\theta ja}$denotes the thermal resistance from the chip die surface to the ambient environment. Its definition can be expressed by the formula:

$$R_{\theta ja} = \frac{T_j - T_a}{P} (°C/W)$$

- Typically, the power dissipation of a chip can be calculated using the formula P= U∗I based on its operating voltage and current. Combined with the chip's thermal resistance parameters and ambient temperature, this allows for an approximate calculation of the chip's junction temperature. This information is then used to design a suitable thermal management solution for the device. As shown in the figure, this is a schematic diagram of the thermal resistance for a surface-mount chip on a board. Heat transfer from the die to the surrounding environment or air occurs through two pathways: the thermal interface between the die and the package case, and the thermal interface between the case and the air. The thermal resistance between the die and the package case is denoted as $R_{\theta jc}$. Typically, for packages with pins, the reference measurement point for case temperature is located at pin 1, which extends from the plastic package.

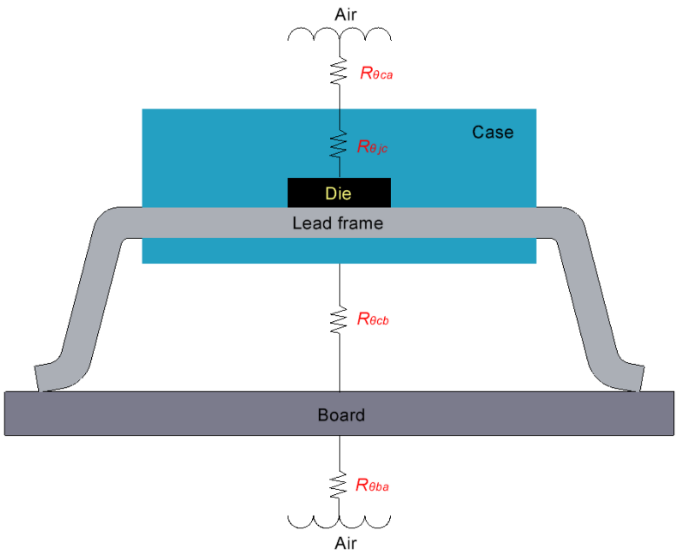


Figure 4.1 Schematic diagram of the structure

- In integrated path current sensor applications, the primary frame carries the measured high current. During normal chip operation, the die is not the primary heat source; the main heat source is the current path—the primary frame. Due to the product's unique characteristics, it is more reasonable to calculate the junction temperature using the thermal resistance $R_{\theta jl}$ between the primary lead and the die. For GXN series sensors, when measuring $R_{\theta jl}$ and $R_{\theta jc}$ parameters, the reference measurement point is the primary side pad. Typically, thermal imaging cameras, thermocouples, or temperature ICs can be used to measure the temperature of the primary side pad. The heat dissipation at this point is not solely the power consumption of the die during operation, but rather the sum of the heat generated by the current flowing through the primary side copper bus and the power dissipation of the die. For example, when using the GXN SOW16 series in an application with 30A current flowing through the primary side during operation, the heating power on the primary copper busbar is $P_L = I_p^2 * R = (30\text{A})^2 \times 0.85\text{m}\Omega$. The heating power of the die during operation is $P_w = V_{CC} * I_{CC}$. Therefore, the junction temperature can be calculated using the formula: $T_j = T_{lead} + R_{\theta jl} * Power = T_{lead} + R_{\theta jl} * (P_L + P_W)$

5 Thermal Evaluation Experiment

5.1 Thermal Evaluation Experiment for SOIC16 Applications

- The copper area on the GXN ANC SOIC16 package demo board measures 21mm × 18mm, approximately 380 mm². Of course, larger copper areas can be used in actual applications to enhance heat dissipation. Here, a very small copper area is used to illustrate a relatively severe scenario. With 2oz copper thickness on both top and bottom layers, under this layout, the chip surface temperature after 30 minutes and 35A current stabilization is shown in the lower right diagram, with the highest point reaching approximately 70℃. This performance is achieved thanks to the package material's excellent thermal conductivity and the copper frame.

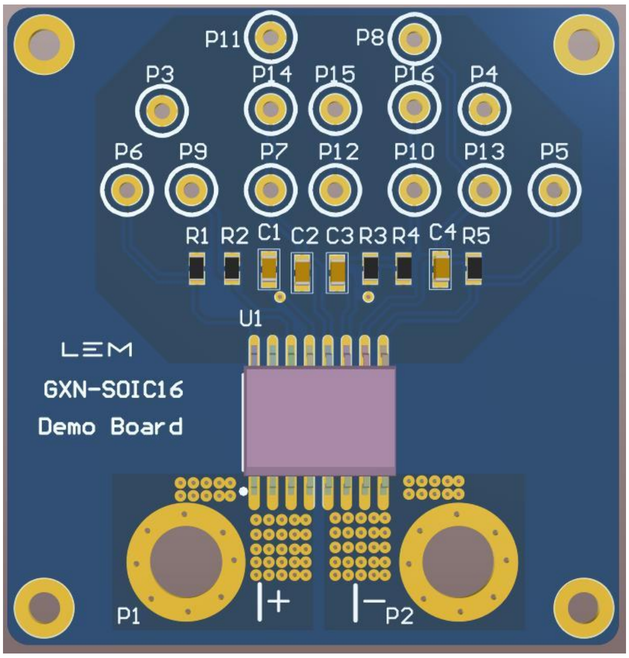


Figure 5.1 GXN ANC_SOIC16 Package PCB Layout

- At room temperature, measure the temperature rise of SOIC16-packaged current sensors under different currents to determine the relationship between junction temperature and time.

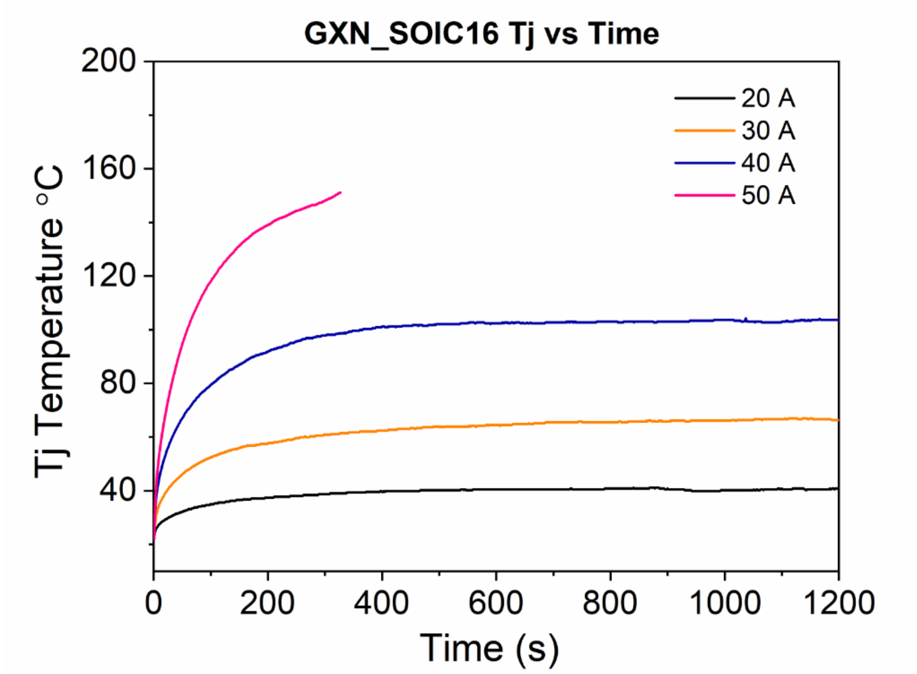


Figure 5.2 GXN ANC_SOIC16 Tj Curves at Different Currents

- The junction temperature rise data under different currents was fitted to derive a junction temperature prediction function for various current levels. Given the primary-side current magnitude, the junction temperature rise can be calculated to estimate junction temperatures across diverse applications, thereby guiding the thermal design of SOW16 packages.

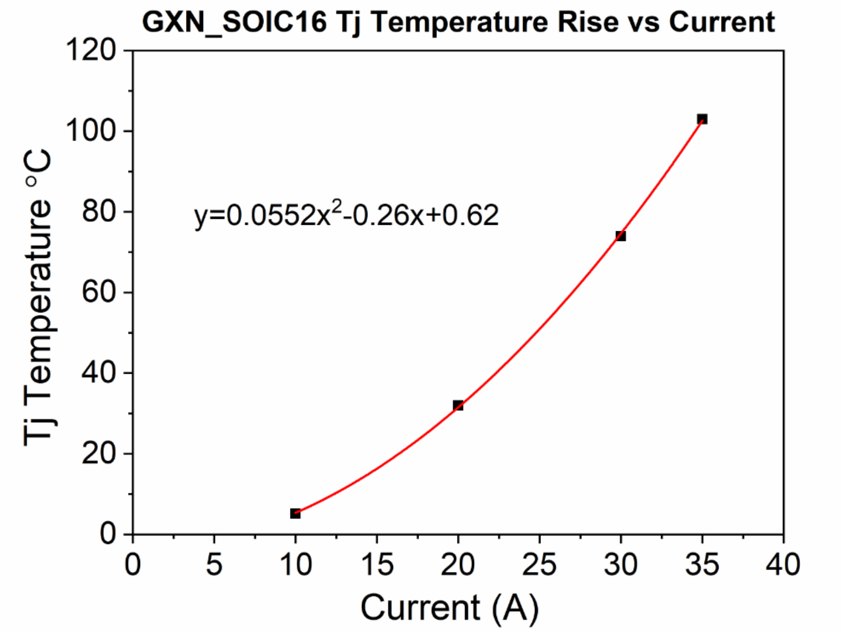


Figure 5.3 GXN ANC_SOIC16 Predictive Function for Tj Curves at Different Currents

5.2 Thermal Evaluation Experiment for SOIC8 Applications

- Based on the demo board using the GXS ANF _SOIC8 package, the junction temperature curve and junction temperature rise prediction curve for the SOP8 package were measured.

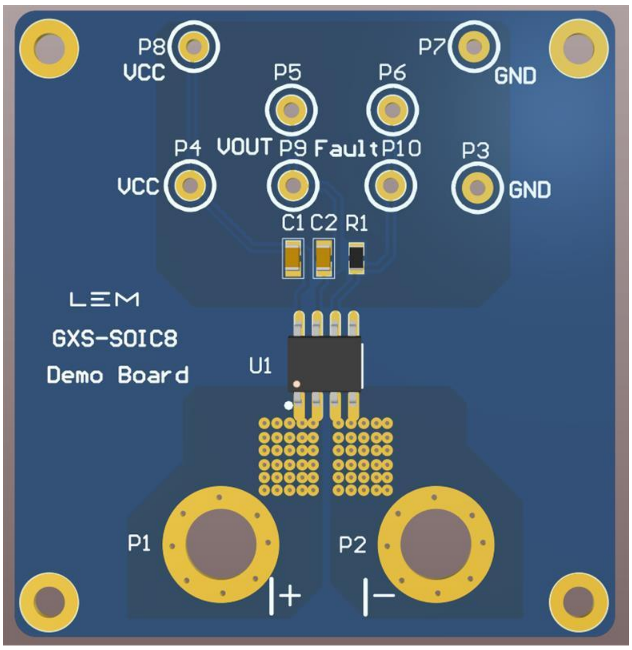


Figure 5.4 GXS ANF_SOIC8 Package PCB Layout

- Testing the temperature rise of current sensors in SOIC8 packages at different currents under ambient conditions, measuring the relationship between junction temperature and time.

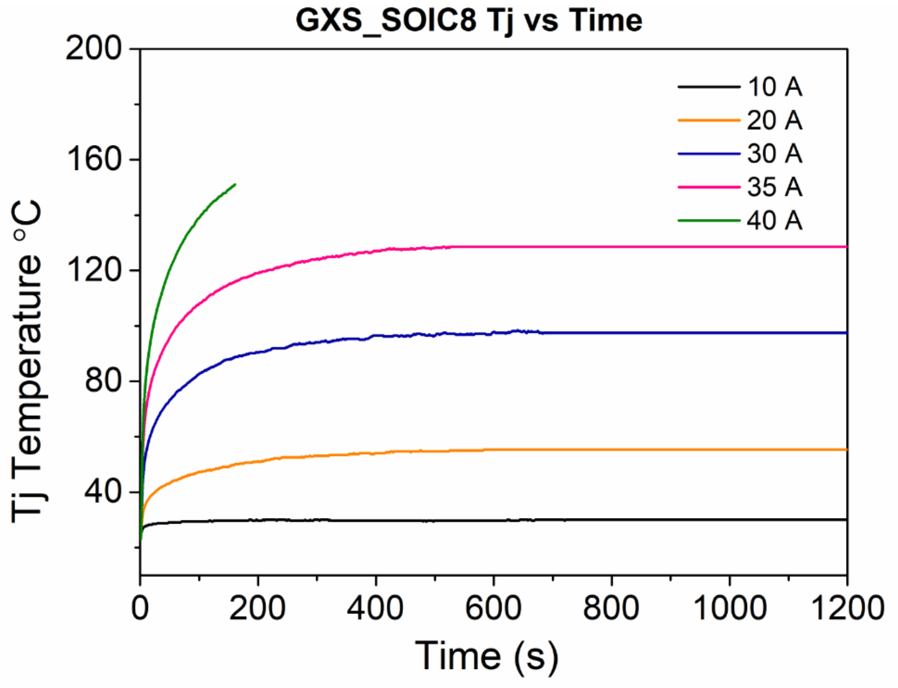


Figure 5.5 GXS ANF_SOIC8 Tj Curves at Different Currents

- The junction temperature rise data under different currents was fitted to derive a junction temperature prediction function for various current levels. Given the primary-side current magnitude, the junction temperature rise can be calculated to estimate junction.

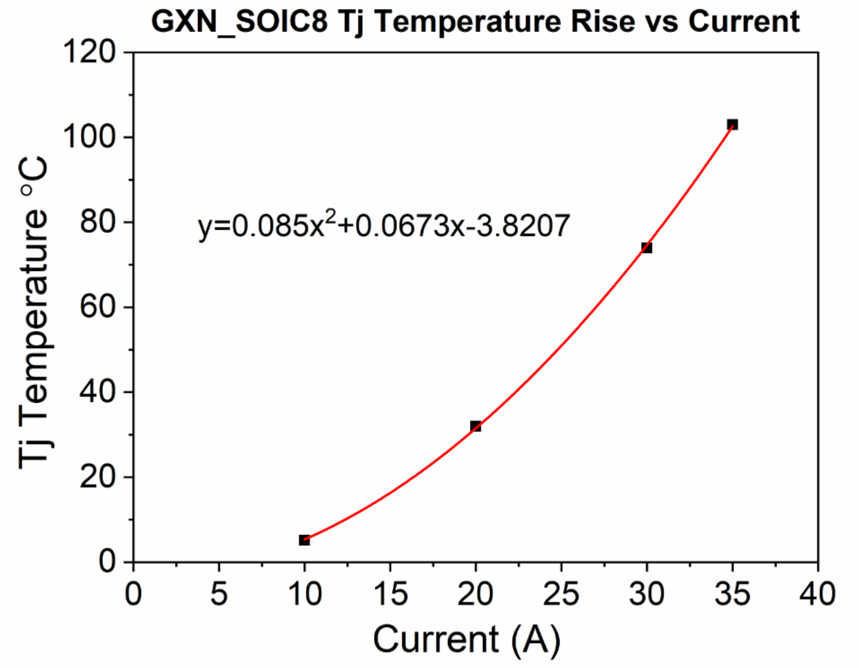


Figure 5.6 GXS ANF_SOIC8 Predictive Function for Tj Curves at Different Current

- The following plots show an example of different thermal responses of the GXS_SOIC8 transducer when used on a LEM evaluation board described on later paragraph

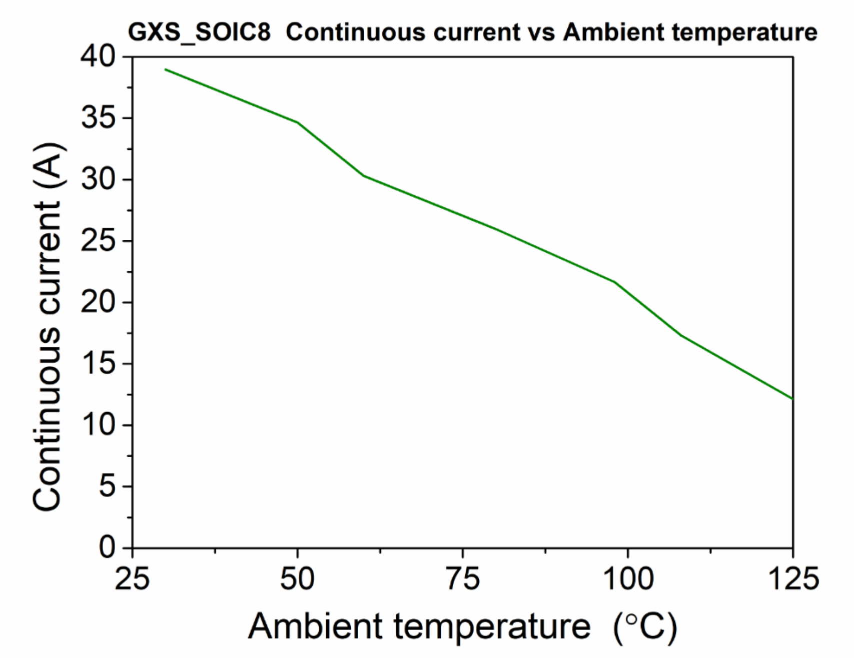


Figure 5.7 GXS _SOIC8 -Derating Curves

The graph shows the mechanical capability of the GXS_SOIC8 package. The maximum current measurement range of the product is limited at 40 A. The maximum temperature should be evaluated on the final system where the current transducer is integrated into the real application. This temperature should never exceed the maximum junction temperature as shown on the previous paragraphs.

6 Optimizing heat dissipation design actions

- A well-designed thermal management system is crucial for ensuring optimal product performance. Typically, optimization can be achieved through several key aspects: copper plating, copper thickness, thermal pads, PCB layout, and heat sinks. Specific details are outlined below.

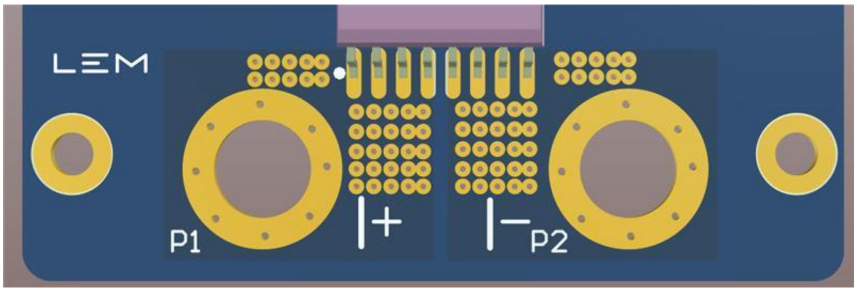
6.1 Optimal Thermal Layout

- A well-designed PCB layout minimizes thermal coupling between components, thereby enhancing overall thermal efficiency. Generally, high-heat-dissipation components on the PCB should be spaced as far apart as possible. This increases the PCB area available for each component to dissipate heat, thereby accelerating cooling. Avoid placing tall components near high-heat-dissipation components to prevent obstructing their heat dissipation pathways.

6.2 Add heat sink pads and through-holes

- Heat dissipation vias along current paths serve as critical “thermal bridges” connecting the PCB's multi-layer copper foils. They efficiently transfer heat from surface copper layers to inner layers and the rear copper plane, forming a three-dimensional heat dissipation network.

Therefore, adding a reasonable number of vias can significantly enhance thermal dissipation efficiency.



6.3 Apply copper over the largest possible area

- In practical applications, the surface layer and bottom layer copper foil of a PCB serve as the primary pathways for heat conduction outward. A larger copper foil area allows heat to diffuse over a broader range, reducing the thermal density per unit area. This naturally enhances heat dissipation efficiency and improves overall cooling performance. Generally, copper foil must be continuous without breaks to prevent thermal diffusion from being obstructed by trace segmentation. Therefore, increasing the copper-clad area strengthens the PCB's thermal diffusion foundation.

6.4 Increase the copper thickness of the hardware

- Generally , the thermal resistance calculation formula for a copper plane can be expressed as:

$$R_{\theta CU} = \frac{\frac{1}{\lambda_{CU}} * L}{S}$$

- S represents area, L denotes length, and λ is the thermal conductivity of copper at 4 W/(cm·℃). For a unit area of 1 cm², the thickness of 1 ounce of copper is 0.0035 cm. Therefore, increasing the copper thickness can reduce the thermal resistance of the copper plane. Using 2 ounces of copper instead of 1 ounce halves the thermal resistance per unit area.

6.5 Proper Use of Heat Sinks

- Utilize heat sinks to enhance active thermal conductivity for heat dissipation. Typically positioned atop the chip or on the PCB's reverse side, heat sinks may incorporate suitable thermal interface materials between components. Eliminating air gaps reduces contact thermal resistance, ensuring efficient heat transfer to the heat sink and achieving effective cooling.